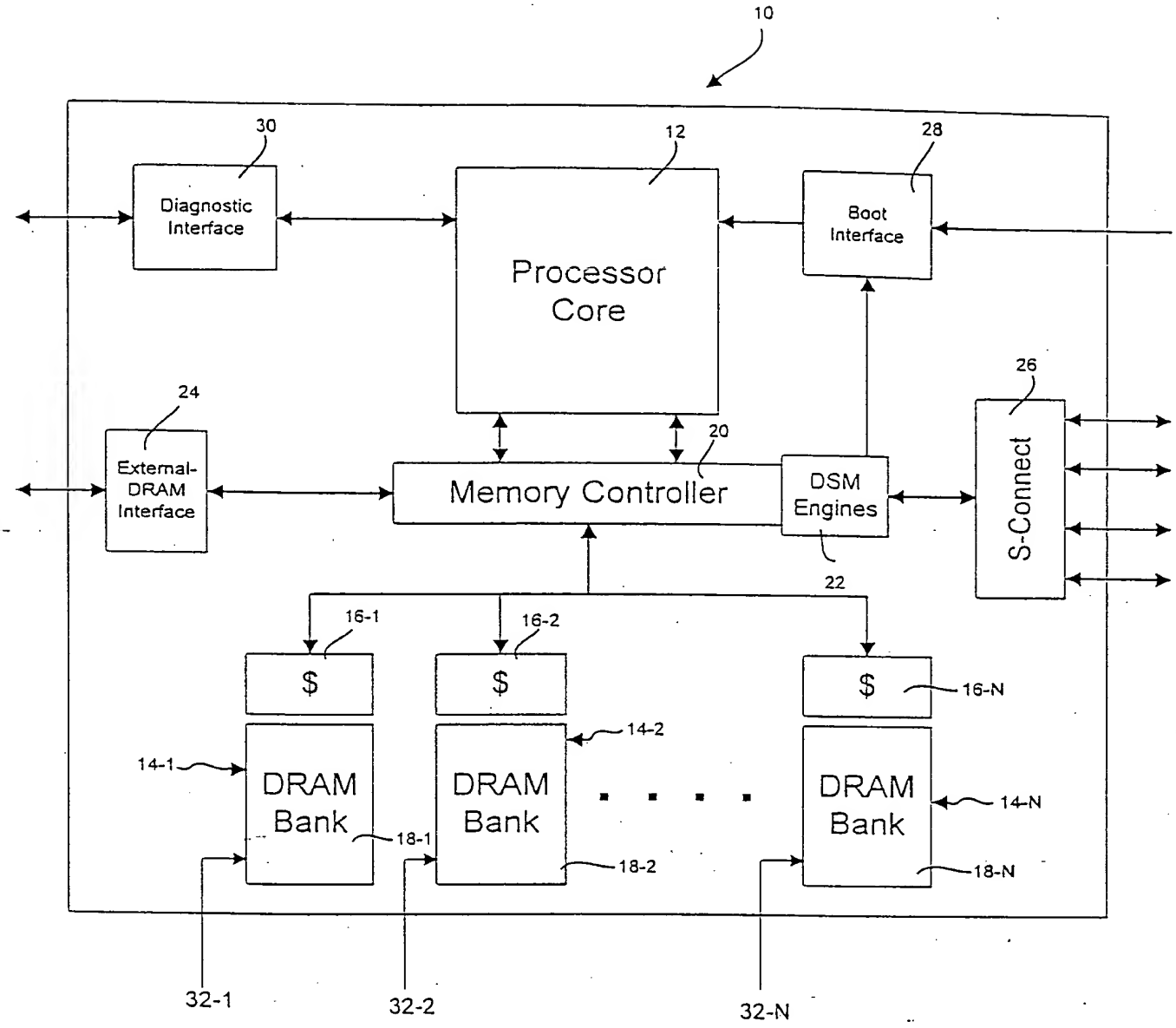

10
30
Diagnostic Interface
12
Processor Core
28
Boot Interface
24
External-DRAM Interface
20
Memory Controller
DSM Engines
26
S-Connect
22
16-1
16-2
$
$
$
16-N
14-1
14-2
DRAM Bank
DRAM Bank
DRAM Bank
14-N
18-1
18-2
18-N
32-1
32-2
32-N

Fig. 1

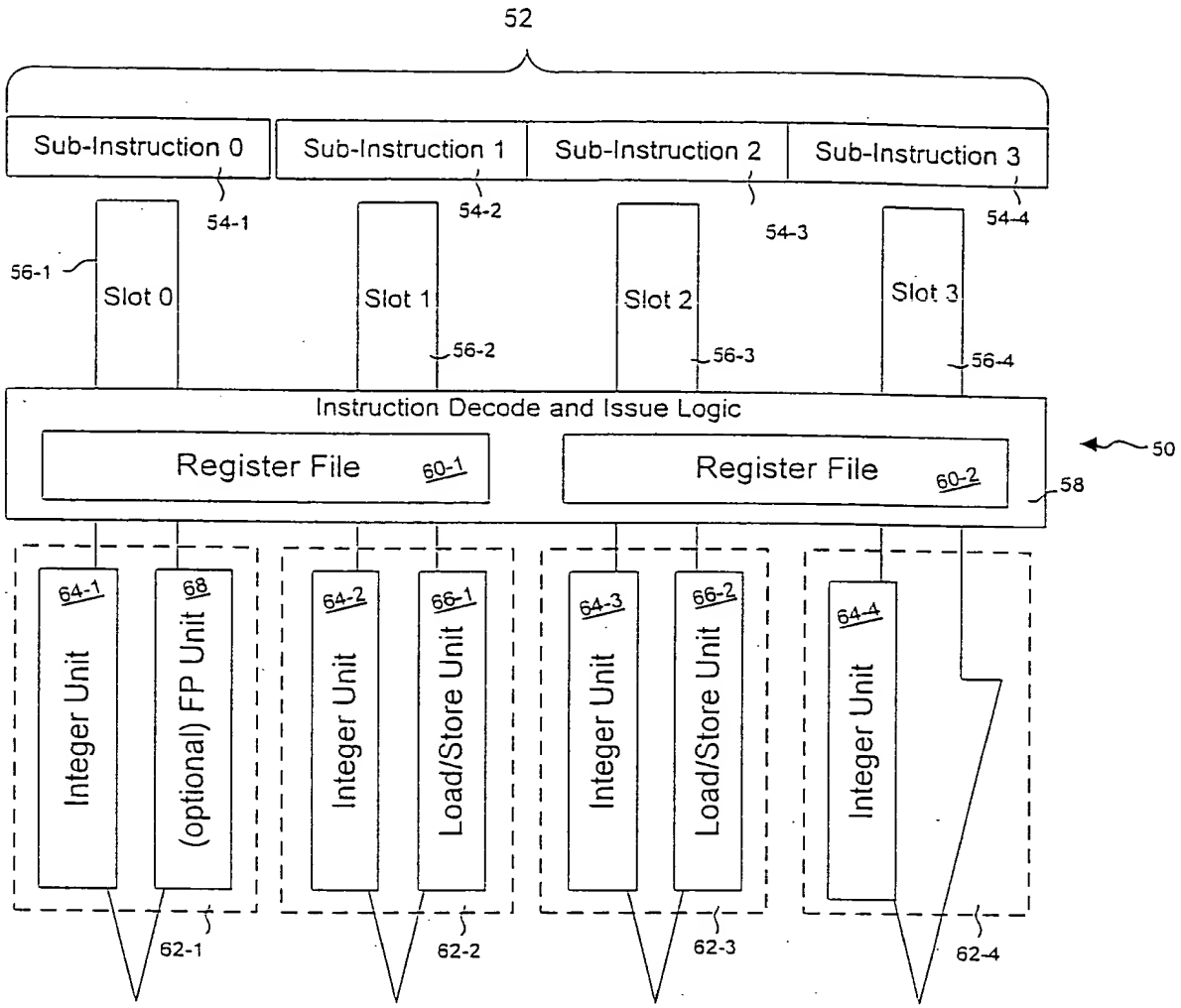

52
Sub-Instruction 0
Sub-Instruction 1
Sub-Instruction 2
Sub-Instruction 3
54-1
54-2
54-3
54-4
56-1
Slot 0
Slot 1
Slot 2
Slot 3
56-2
56-3
56-4
Instruction Decode and Issue Logic
50
Register File 60-1
Register File 60-2
58
64-1
Integer Unit
68
(optional) FP Unit
64-2
Integer Unit
66-1
Load/Store Unit
64-3
Integer Unit
66-2
Load/Store Unit
64-4
Integer Unit
62-1
62-2
62-3
62-4

Fig. 2

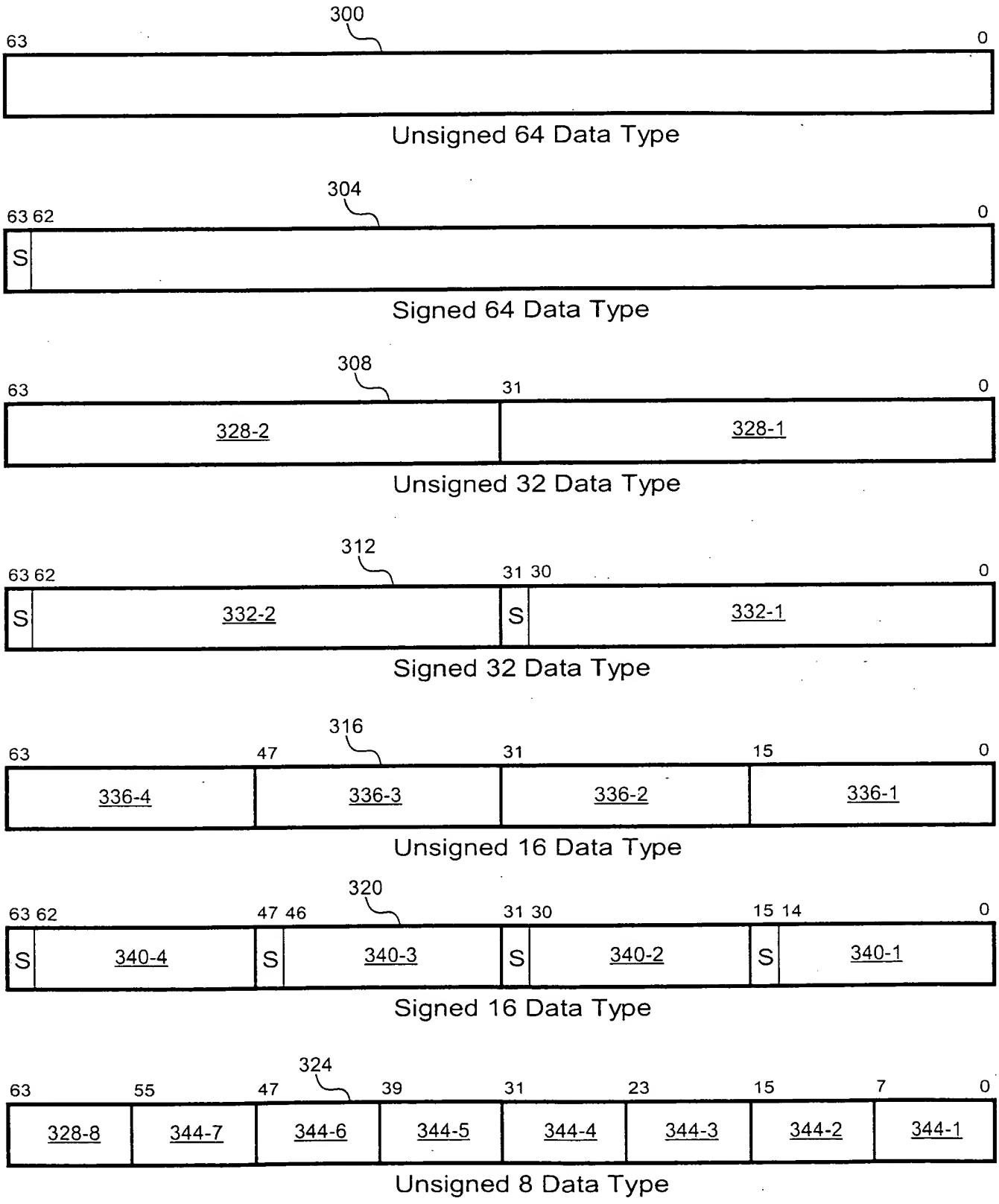
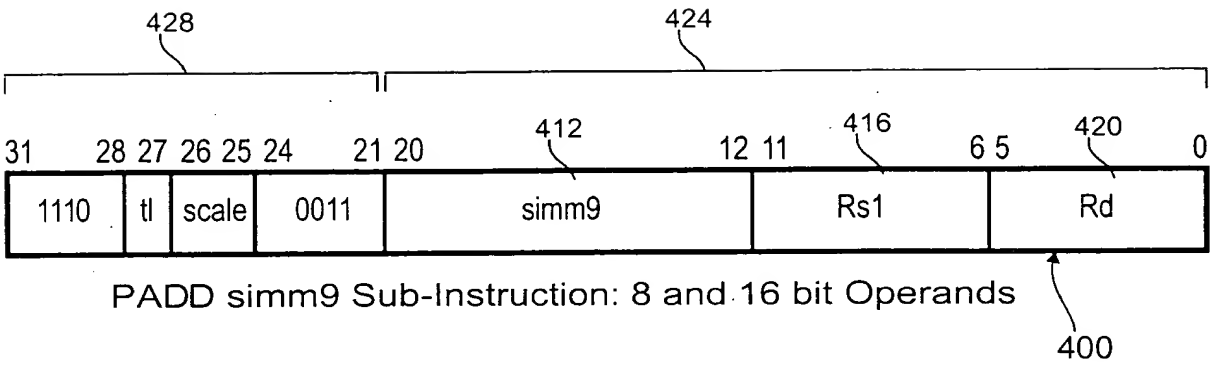
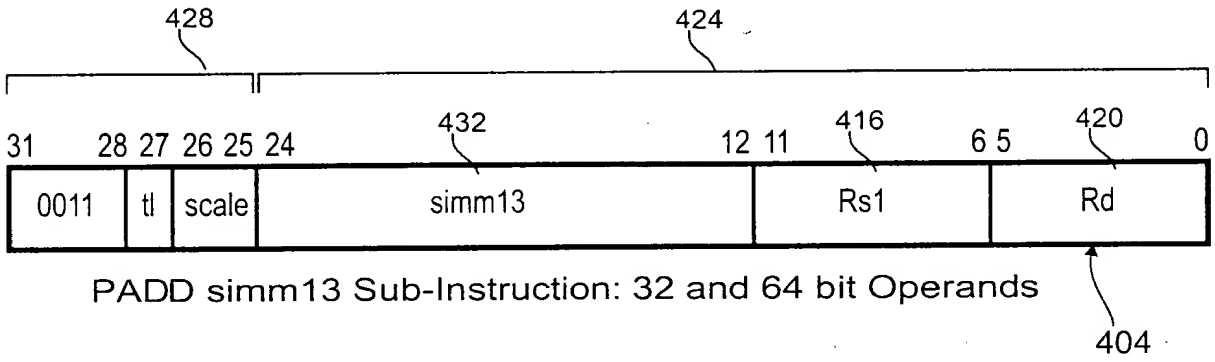

300
63
0
Unsigned 64 Data Type
304
63 62
0
S
Signed 64 Data Type
308
63
31
0
328-2
328-1
Unsigned 32 Data Type
312
63 62
31 30
0
S
332-2
S
332-1
Signed 32 Data Type
316
63
47
31
15
0
336-4
336-3
336-2
336-1
Unsigned 16 Data Type
320
63 62
47 46
31 30
15 14
0
S
340-4
S
340-3
S
340-2
S
340-1
Signed 16 Data Type
324
63
55
47
39
31
23
15
7
0
328-8
344-7
344-6
344-5
344-4
344-3
344-2
344-1
Unsigned 8 Data Type

Fig. 3


428
424
31
28 27 26 25 24
21 20
412
12 11
416
6 5
420
0
1110
tl
scale
0011
simm9
Rs1
Rd
PADD simm9 Sub-Instruction: 8 and 16 bit Operands
400


428
424
31
28 27 26 25 24
432
12 11
416
6 5
420
0
0011
tl
scale
simm13
Rs1
Rd
PADD simm13 Sub-Instruction: 32 and 64 bit Operands
404

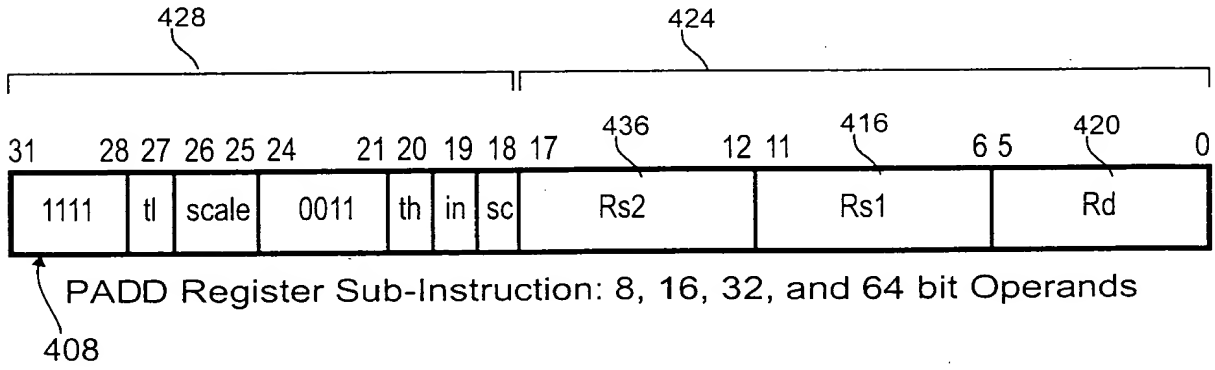

428
424
31
28 27 26 25 24
21 20 19 18 17
436
12 11
416
6 5
420
0
1111
tl
scale
0011
th
in
sc
Rs2
Rs1
Rd
PADD Register Sub-Instruction: 8, 16, 32, and 64 bit Operands
408

Fig. 4

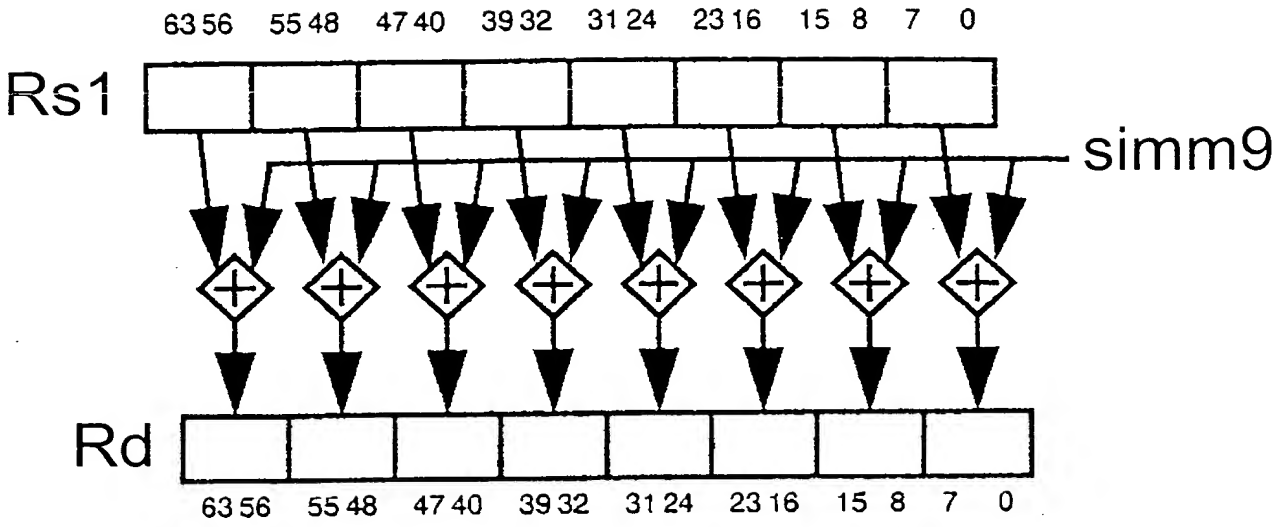

63 56
55 48
47 40
39 32
31 24
23 16
15 8
7 0
Rs1
simm9
Rd

Fig. 5

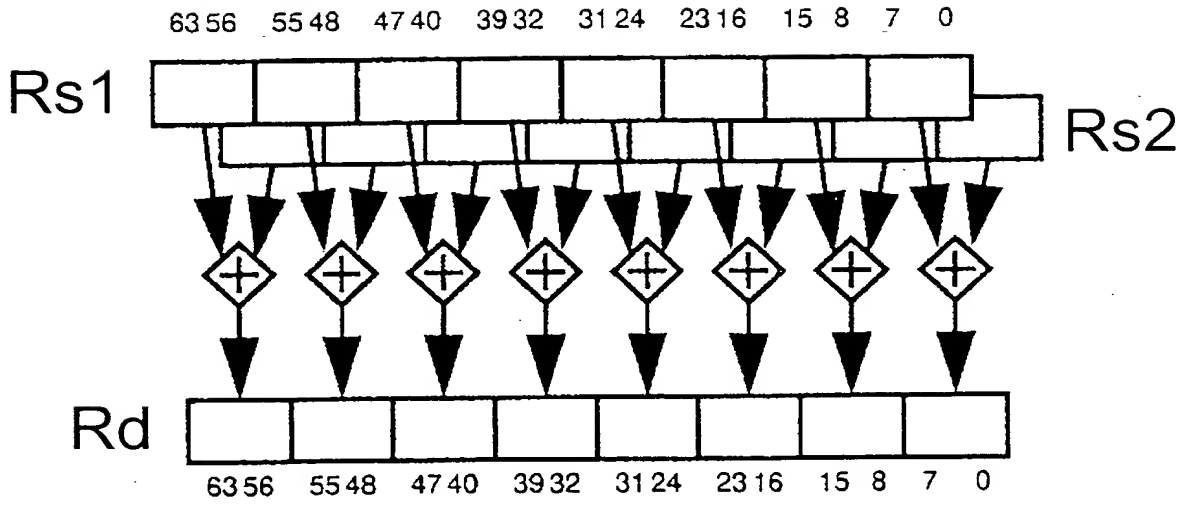

63 56
55 48
47 40
39 32
31 24
23 16
15 8
7 0
Rs1
Rs2
Rd

Fig. 6

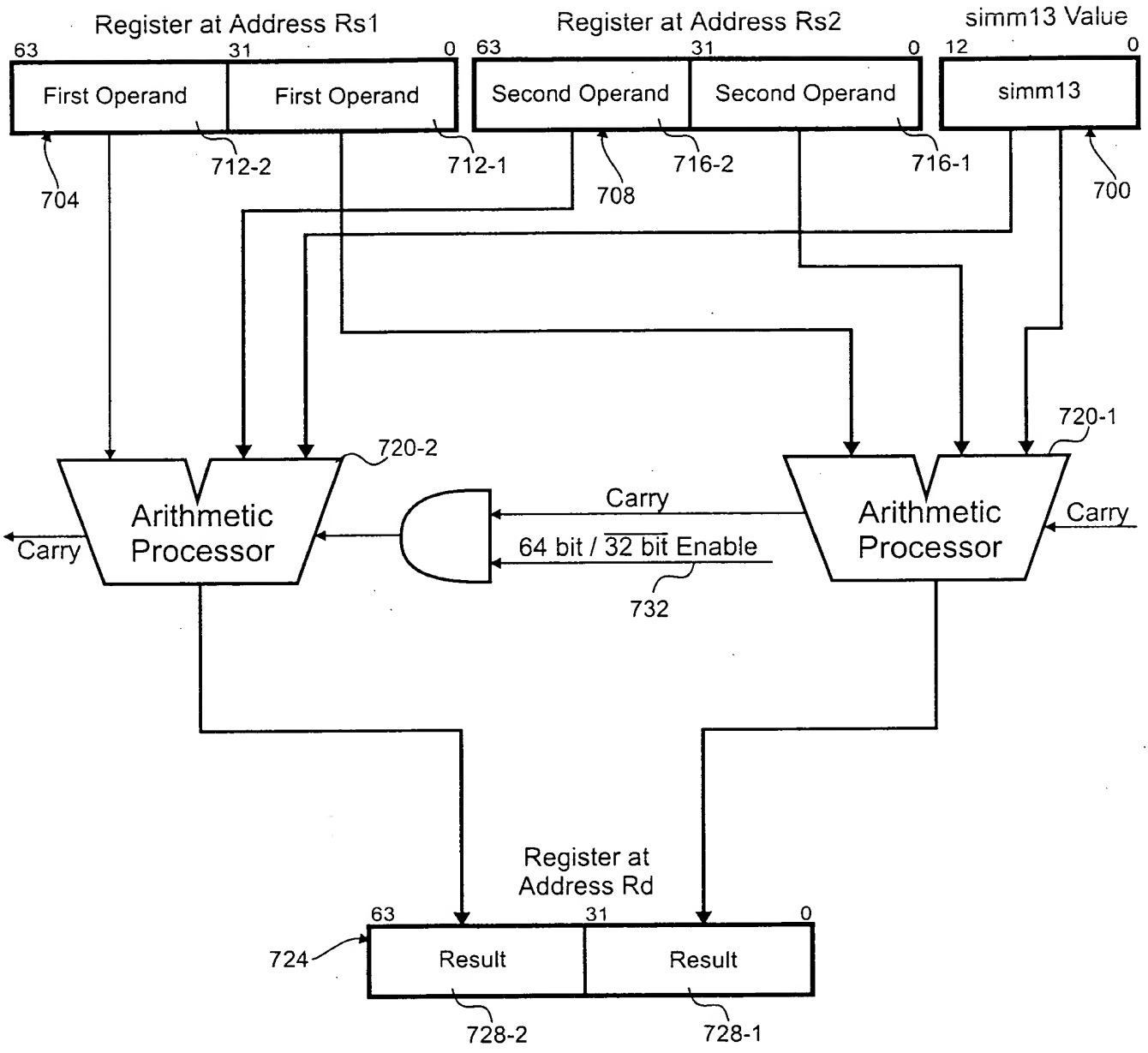

Register at Address Rs1
Register at Address Rs2
simm13 Value
63
31
0
12
First Operand
First Operand
Second Operand
Second Operand
simm13
704
712-2
712-1
708
716-2
716-1
700
720-1
720-2
Arithmetic Processor
Arithmetic Processor
Carry
Carry
Carry
64 bit / 32 bit Enable
732
Register at Address Rd
724
Result
Result
728-2
728-1

Fig. 7

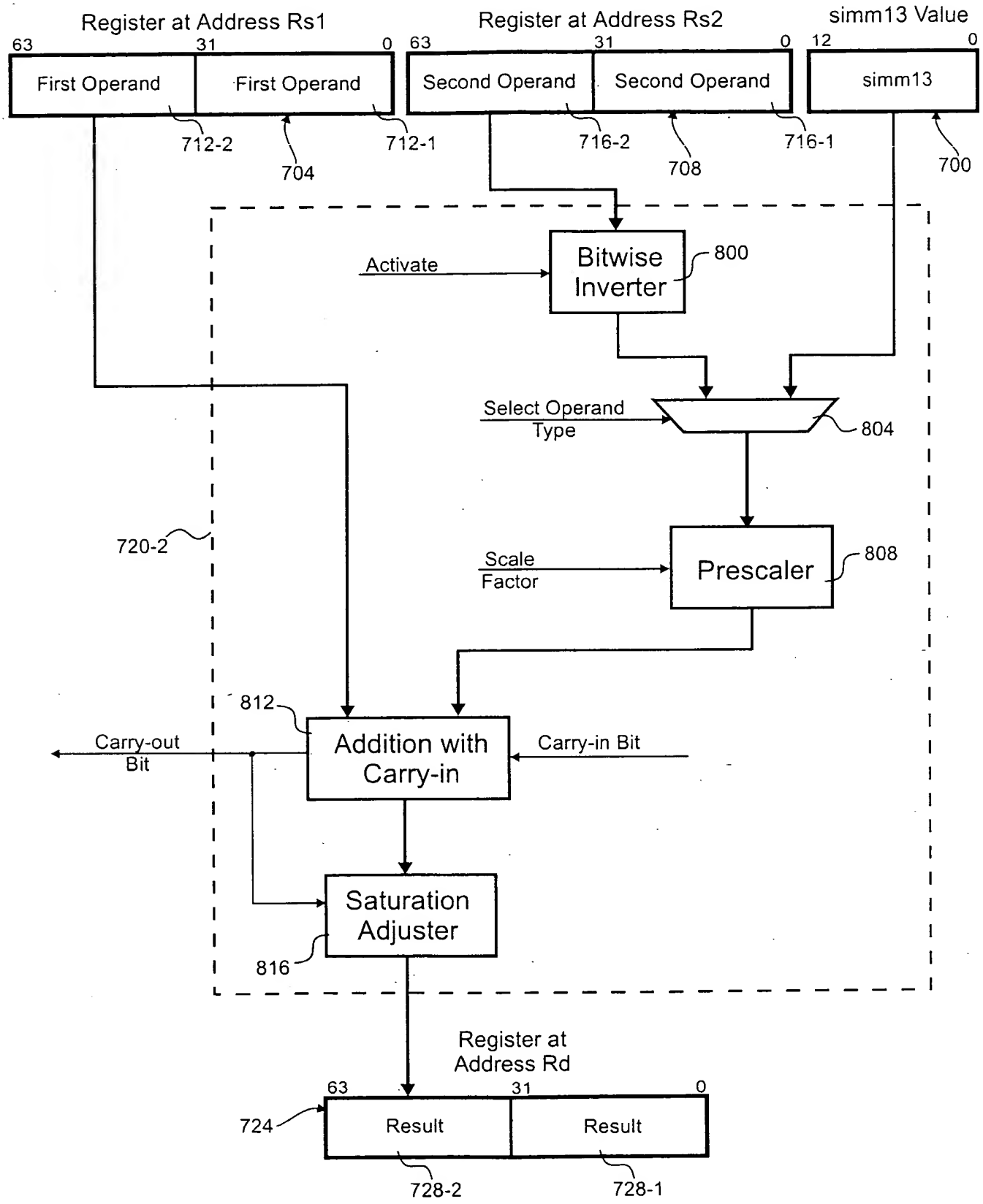

Register at Address Rs1
63
31
0
First Operand
First Operand
712-2
704
712-1
Register at Address Rs2
63
31
0
Second Operand
Second Operand
716-2
708
716-1
simm13 Value
12
0
simm13
700
Activate
Bitwise Inverter
800
Select Operand Type
804
720-2
Scale Factor
Prescaler
808
812
Carry-out Bit
Addition with Carry-in
Carry-in Bit
Saturation Adjuster
816
Register at Address Rd
63
31
0
724
Result
Result
728-2
728-1

Fig. 8A

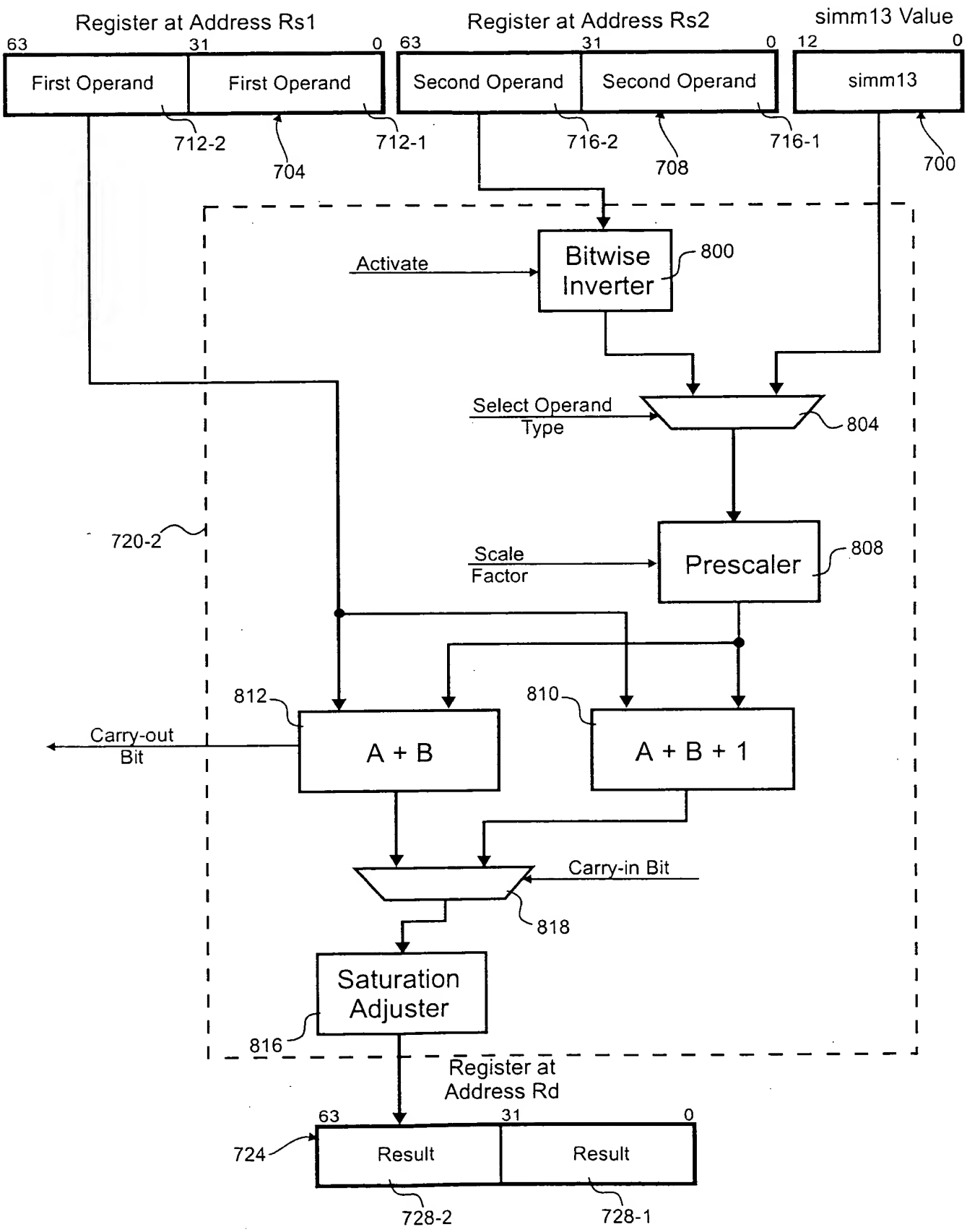

Register at Address Rs1
63
31
0
First Operand
First Operand
712-2
704
712-1
Register at Address Rs2
63
31
0
Second Operand
Second Operand
716-2
708
716-1
simm13 Value
12
0
simm13
700
Activate
Bitwise Inverter
800
Select Operand Type
804
720-2
Scale Factor
Prescaler
808
812
810
Carry-out Bit
A + B
A + B + 1
Carry-in Bit
818
Saturation Adjuster
816
Register at Address Rd
63
31
0
724
Result
Result
728-2
728-1

Fig. 8B

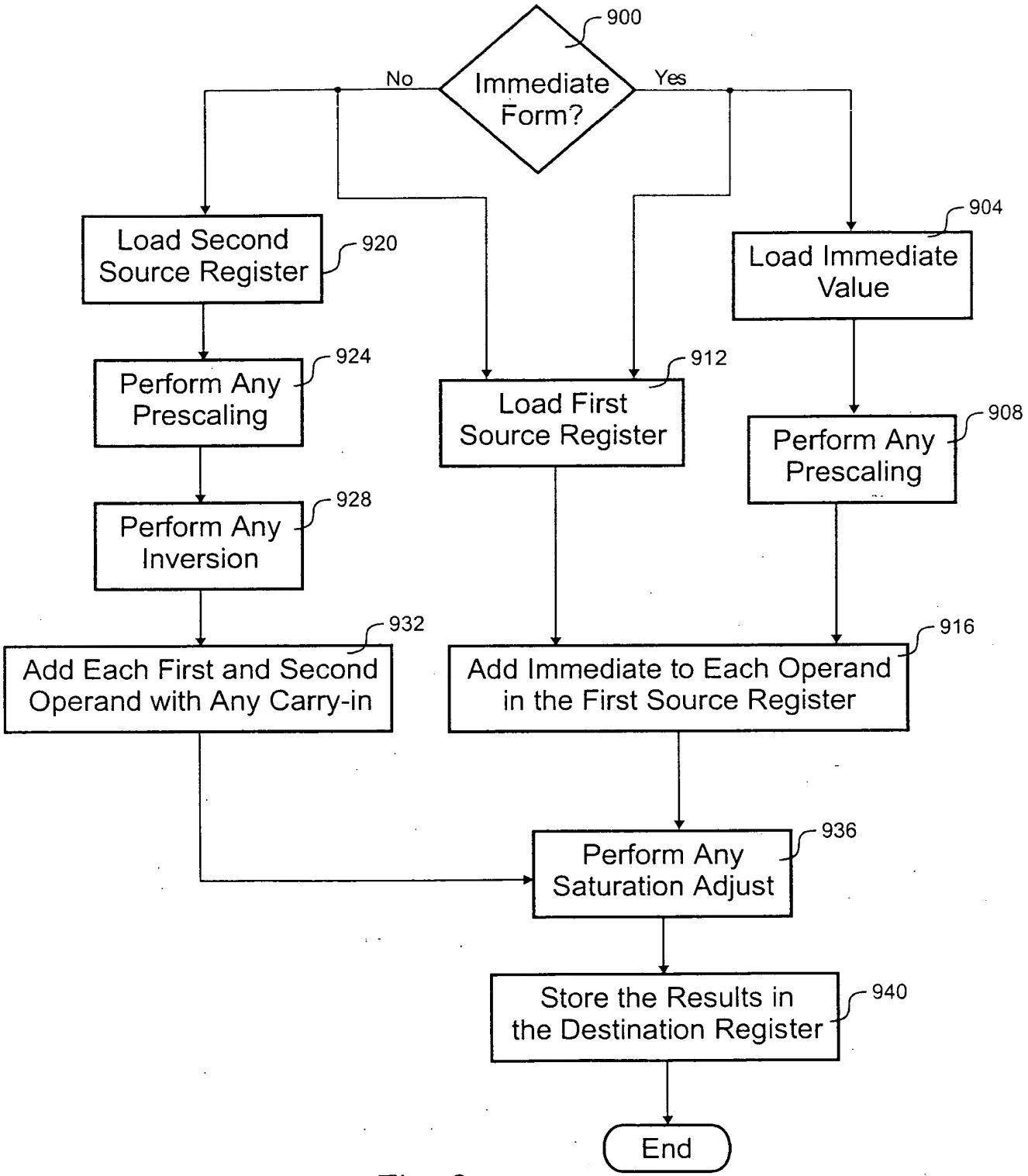

900
Immediate Form?
No
Yes
Load Second Source Register
920
Load Immediate Value
904
Perform Any Prescaling
924
Load First Source Register
912
Perform Any Prescaling
908
Perform Any Inversion
928
Add Each First and Second Operand with Any Carry-in
932
Add Immediate to Each Operand in the First Source Register
916
Perform Any Saturation Adjust
936
Store the Results in the Destination Register
940
End

Fig. 9